AN2583
Application note

Understanding and applying the M41T00AUD real-time clock with audio

Introduction

Drawing on the fact that the squarewave generator built in to many ST serial RTCs can be used as a tone generator, users have been employing ST real-time clocks in printer-fax scanner units for several years. In these applications, the squarewave output is used to create the audible beeps these all-in-one (AIO) machines make when a key is pressed or an error occurs.

The beep signals drive an amplifier circuit which in turn drives a speaker. Furthermore, other tone sources from within the AIO also go to the speaker, so they are summed into the amplifier along with the squarewave signal. One of these sources is the phone line. It is audible while the fax is dialing and negotiating the connection.

Additionally, it is necessary to control the gain of the amplifier and to limit the bandwidth of the audio signal, so some form of volume control and filtering is required.

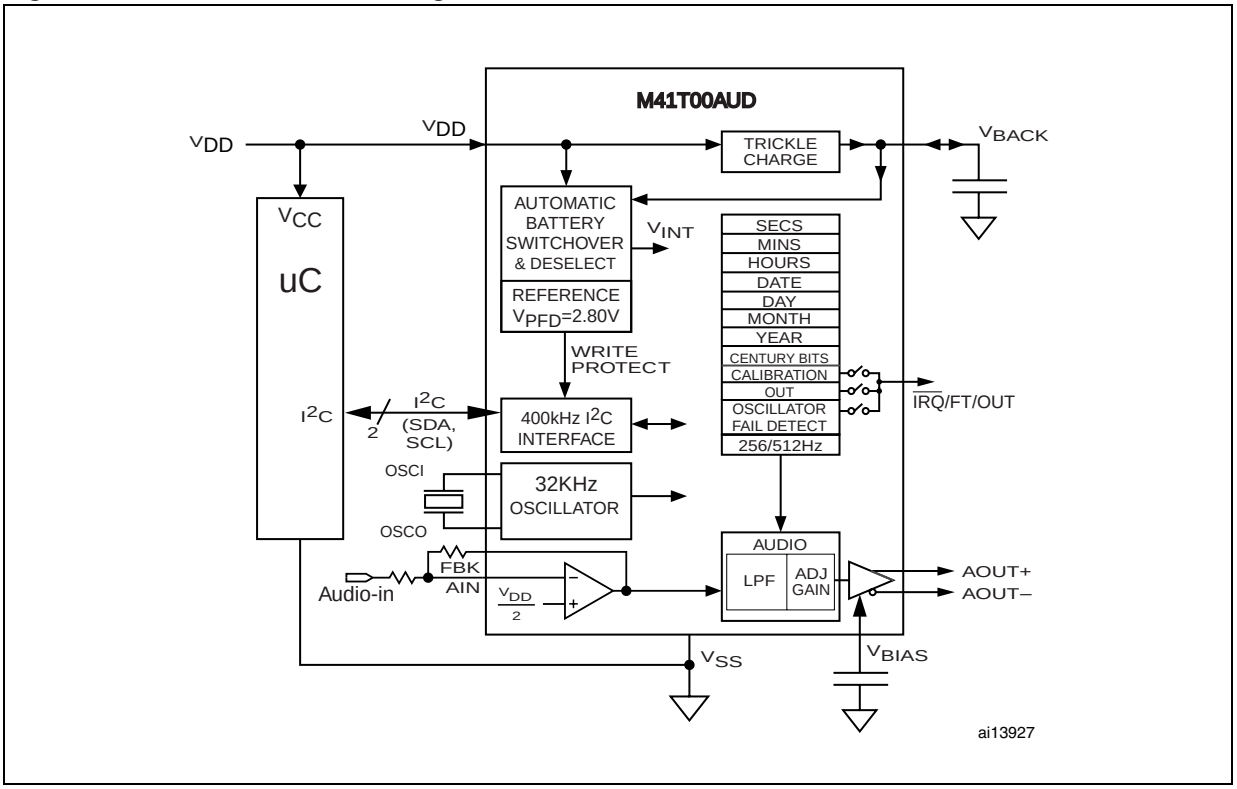
As a result, ST developed the M41T00AUD which combines a real-time clock with an audio section. Referring to *Figure 1 on page 2*, the clock is based on ST's M41T00 and includes several enhancements such as a trickle charge circuit for charging backup capacitors and a voltage reference for precisely controlling the backup switchover threshold.

The audio section starts with an input amplifier for summing multiple signals of varying levels. Next is an 8 kHz low-pass filter, then a 16-step, digitally controlled gain stage with 3 dB steps. Finally, the output section is a bridged amplifier capable of driving 300 mW into an 8 Ω load (with V_{CC} at 3.3 V).

Thus, the M41T00AUD is a highly integrated circuit perfect for All-In-One printer applications, as well as other consumer devices, where high functionality and low cost are key requirements.

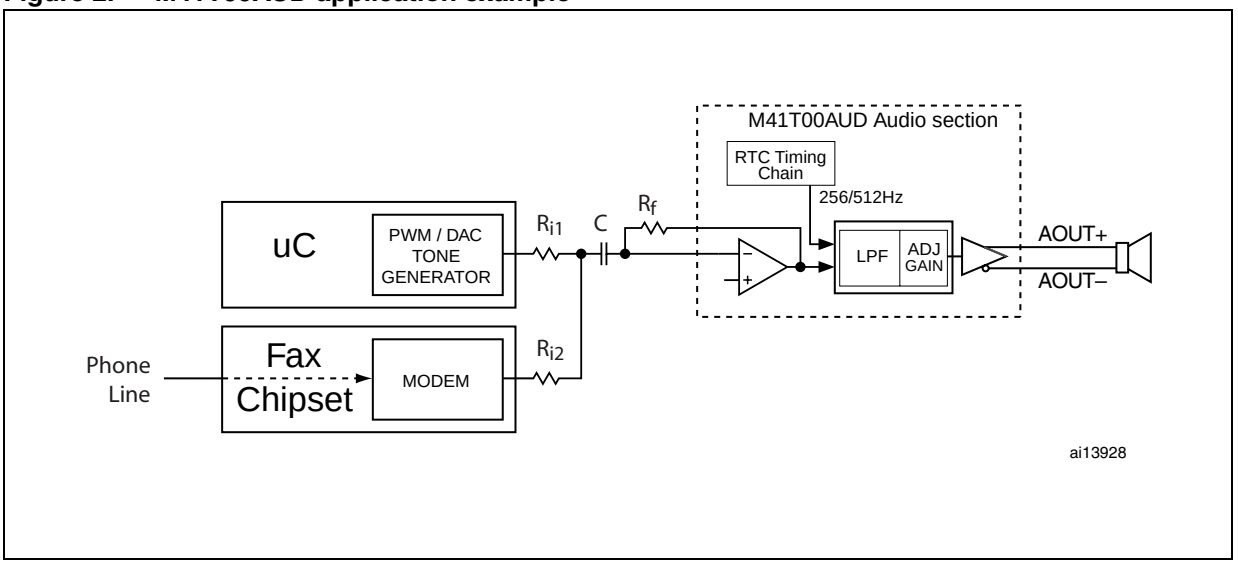
1 Typical application

Figure 1. M41T00AUD block diagram



The typical AIO application has audio sources in the system micro-controller and in the fax chipset originating with the phone line. These are summed into the input amplifier which in turn drives the filter along side the internally generated 256/512 Hz tones (see *Figure 2*).

Figure 2. M41T00AUD application example



Input resistors, R_{in}, along with the feedback resistor, R_f, control the gain into the part. Each input can be added at a different level by changing its corresponding input resistor thus allowing signals of varying levels to be normalized.

The input capacitor, C, blocks any DC into the part. Since the M41T00AUD uses a single supply, its internal mid-point is $V_{DD}/2$ and not ground. Thus, input signals would need to be centered at $V_{DD}/2$ to connect directly. Otherwise, the coupling capacitor is necessary. Furthermore, it provides an input filter blocking low frequencies. When R_{in} = 20 kΩ and C = 0.1 uF, signals below approximately 80 Hz will be attenuated.

After the input amplifier is the low-pass filter with its knee at 8 kHz. With the input capacitor, these form a band pass filter over the range of 80 Hz to 8 kHz.

Also input to the LPF is the 256/512 Hz signal from the RTC timing chain. Software controls whether it is passed into the LPF and which of the two frequencies is selected. Software also controls the gain. A mute bit can be set to shut off all audio and a four-bit GAIN field controls the digital gain stage selecting between –33 dB and +12 dB of gain in 3 dB steps.

The output is a bridged amplifier capable of sinking/sourcing over 300 mA. For V_{CC} = 3.3 V, it can readily drive over 300 mW of power into an 8 Ω speaker.

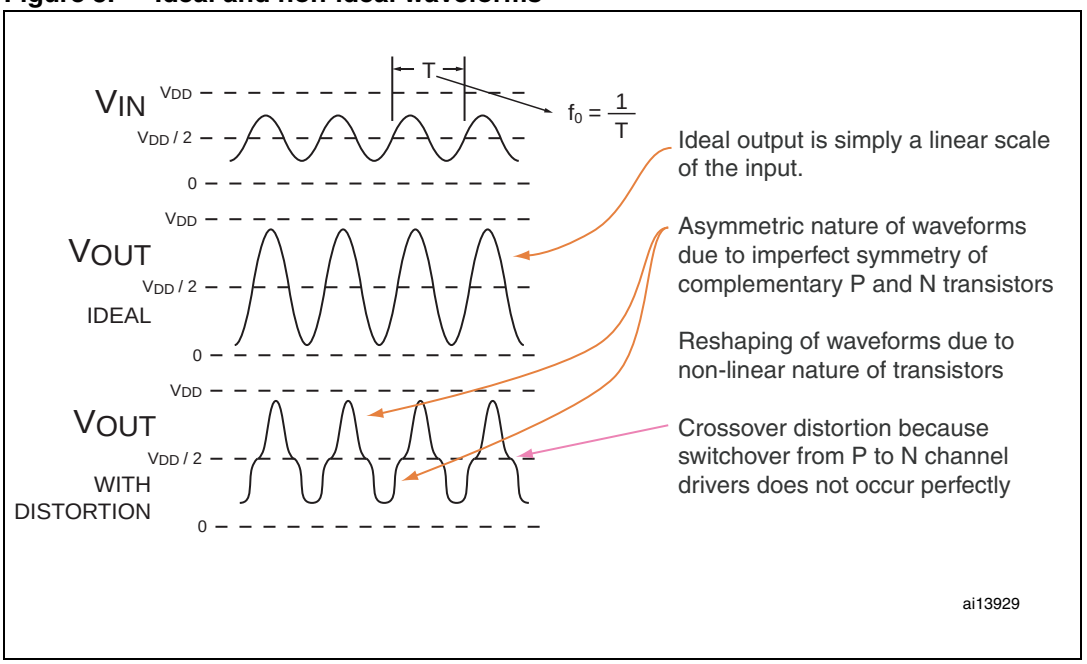
2 Audio characteristics

Several parameters are used to characterize amplifier circuits. Among them are gain, total harmonic distortion, power-supply rejection ratio and output power. The following is a brief primer on these topics.

2.1 Harmonic distortion

Ideally, the output of an audio amplifier is a linear reproduction of its input; the output differs only in amplitude and is identical in all other respects.

Figure 3. Ideal and non-ideal waveforms



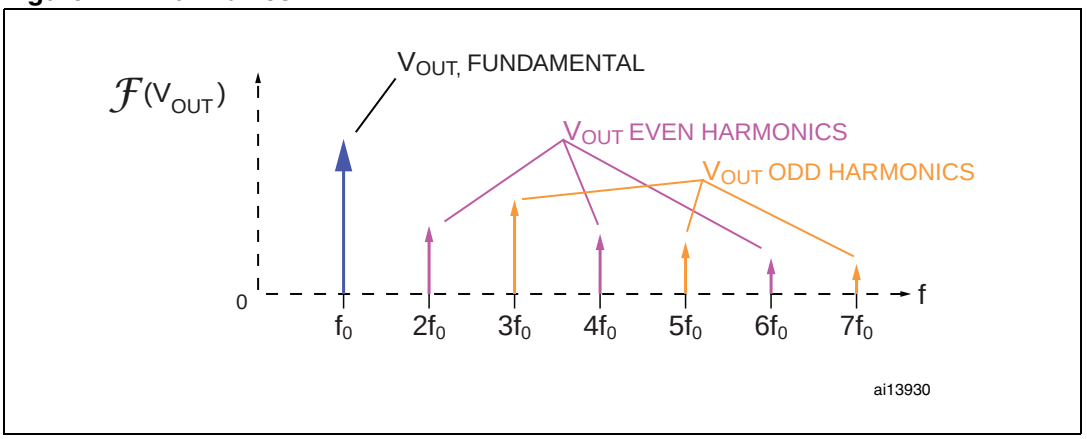
In reality, several things combine to distort the waveform resulting in the addition of harmonics in the output, as depicted in *Figure 4*. The amplifiers are not perfectly linear, so some reshaping of the waveform will occur. This happens in a symmetric fashion resulting in the addition of odd harmonics.

The crossover point at which one drive transistor turns on and the other turns off is imperfect and results in crossover distortion as shown in *Figure 3* (exaggerated for effect). This too adds odd harmonics.

The lack of perfect symmetry in the complementary output transistors will cause the top and bottom halves of the waveforms to be asymmetric resulting in even harmonics.

The result is that the amplifier output will contain several artifacts not present in the input.

Figure 4. Harmonics



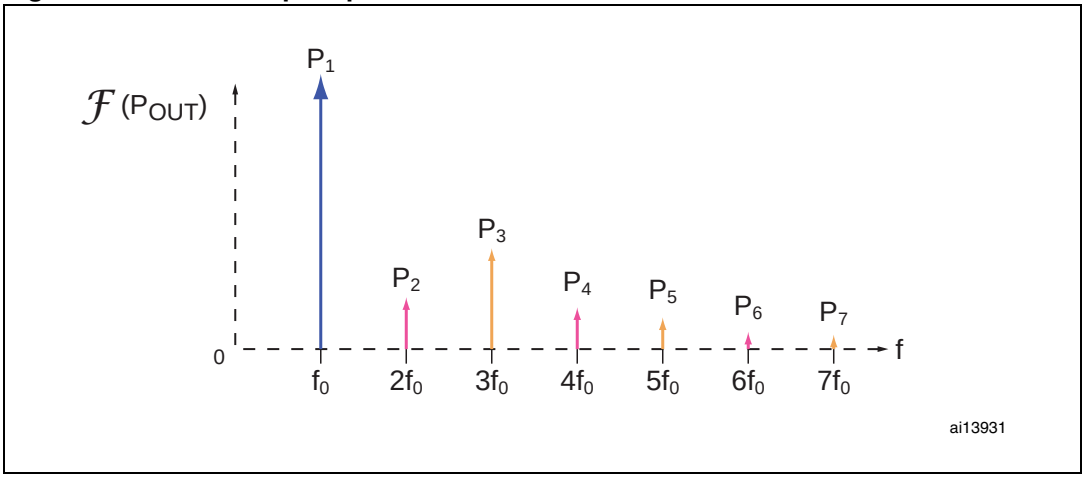
2.1.1 Total harmonic distortion

The Total Harmonic Distortion, THD, is a measure of the linearity or purity of the amplification process and indicates to what extent the artifacts occur. A pure sine wave is input to the amplifier and the spectrum of the output is determined. The THD figure is a comparison of the output power or voltage levels of the harmonics to the fundamental.

Figure 5 illustrates an example output spectrum. P_1 is the fundamental frequency while P_2 to P_7 are the harmonics.

The THD figure establishes the fraction of the output signal which is harmonics.

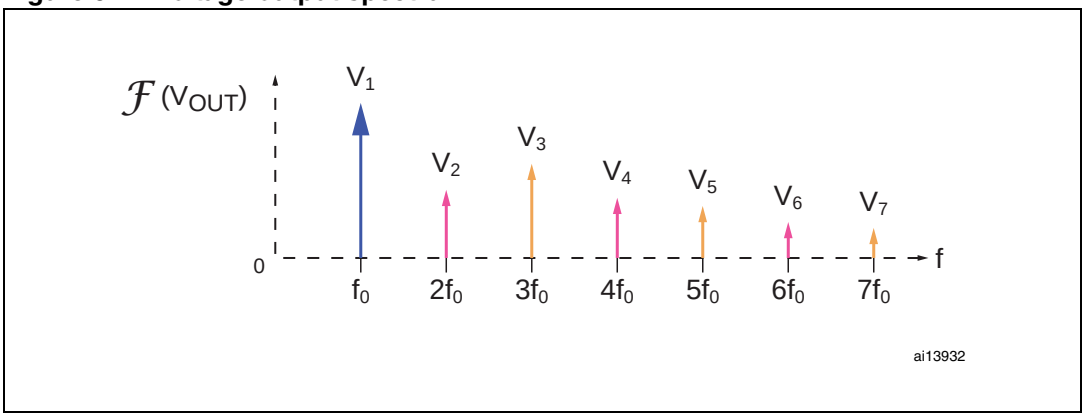
Figure 5. Power output spectrum



There are two methods used to calculate the THD. The first method compares the power of the harmonics to the fundamental.

$$THD_P = \frac{\sum \text{harmonic powers}}{\text{power of fundamental frequency}} = \frac{P_2 + P_3 + P_4 + P_5 + P_6 + P_7 + \cdots}{P_1}$$

Figure 6. Voltage output spectrum



The other THD calculation method compares the voltages.

$$THD_V = \frac{\sqrt{\sum (\text{harmonic voltages})^2}}{\text{voltage of fundamental frequency}} = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2 + \cdots}}{V_1}$$

Since P is proportional to V_2, this second method amounts to being the square root of the first.

$$THD_V = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2 + \cdots}}{V_1} = \frac{\frac{1}{\sqrt{R}}}{\frac{1}{\sqrt{R}}} \cdot \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 +}}{V_1}$$

$$= \frac{\sqrt{\frac{V_2^2}{R} + \frac{V_3^2}{R} + \frac{V_4^2}{R} + \frac{V_5^2}{R} + \frac{V_6^2}{R} + \frac{V_7^2}{R} \cdots}}{\frac{V_1}{\sqrt{R}}} = \frac{\sqrt{P_2 + P_3 + P_4 + P_5 + P_6 + P_7 + \cdots}}{\sqrt{P_1}}$$

$$THD_V = \sqrt{THD_P}$$

Because THD is generally a number less than 1, THD_V, being the square root of THD_P , will be a larger number than THD_P .

The required THD specification for the M41T00AUD is less than 2% at 1 kHz and 300 mW. The voltage formula was used in the measurement for this, and makes for the more difficult specification since it tends to yield the higher number.

Example: Let V_1 = 1 V, V_2 = 0.1 V, V_3 = 0.08 V, V_4 = 0.06 V and V_5 = 0.04 V

$$THD_V = \frac{\sqrt{0.1^2 + 0.08^2 + 0.06^2 + 0.04^2}}{1^2} = 0.147 = 14.7\%$$

$$THD_P = THD_V{}^2 = 0.0216 = 2.16\%$$

Thus the voltage formula makes for a more challenging specification.

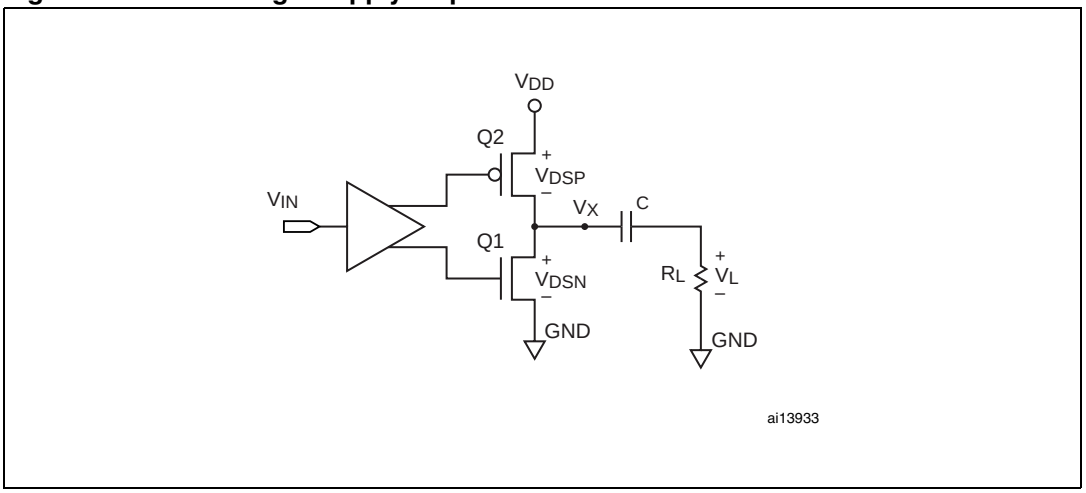
2.2 Amplifier primer

Several types of amplifiers are possible for fabrication in semiconductor ICs. The following is a brief overview of the types and their power capabilities.

2.2.1 Simple amplifier

Figure 7 illustrates a simple amplifier circuit. The input section provides any signal conditioning - gain and offset - necessary for driving the output transistors shown here. The midpoint voltage, V_X, is biased at $V_{DD}/2$. At its maximum, V_X will swing up to $V_{DD} - V_{DSP\text{-}min}$ when Q2 is fully on, and down to $V_{DSN\text{-}min}$ when Q1 is fully on.

Figure 7. Basic single supply amplifier



For the purposes of analysis, we can assume $V_{DSP\text{-}min}$ and $V_{DSN\text{-}min}$ are small compared to V_{DD} and thus ignore them here.

With that in mind, the point V_X will swing between GND (0 V) and V_{DD}.

For audio applications, it is necessary that the output signal be purely AC. There should be no DC component in it. The output signal must swing symmetrically about ground.

Therefore, a capacitor, C, is inserted in series between V_X and the load, R_L. This will have the effect of blocking any DC in the output. So, while the point V_X will swing between V_{DD} and ground, with an average (DC) level of $V_{DD}/2$, the output voltage V_L will swing between $V_{DD}/2$ and $-V_{DD}/2$, with an average of 0V. This assumes no voltage drop across the capacitor. If the capacitance is sufficiently high for the frequency range of interest, then the drop across the capacitor will be small and the assumption valid.

If the signal at V_X is a sine wave swinging between V_{DD} and ground, we can write that as

$$V_X(t) = \frac{V_{DD}}{2} \cdot (1 + \sin \omega t) = \frac{V_{DD}}{2} + \frac{V_{DD}}{2} \cdot \sin \omega t$$

and

$$\omega = 2\pi f$$

where f is the frequency of the sine wave.

The signal at the load then, with the DC component removed, is

$$V_L(t) = \frac{V_{DD}}{2} \cdot \sin \omega t$$

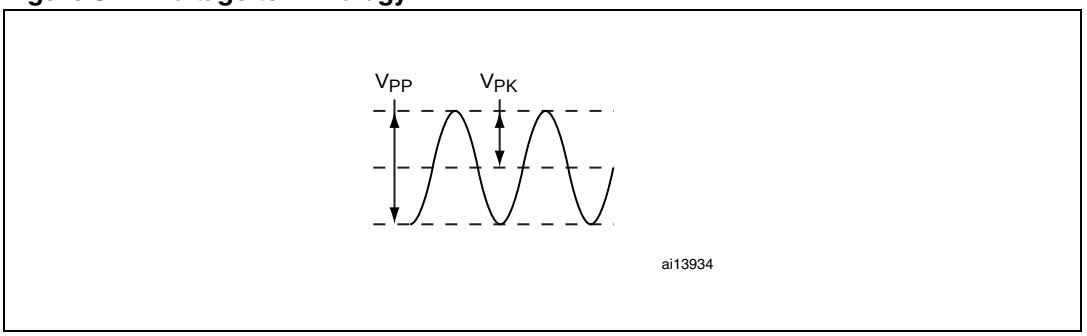
2.2.2 Output power

A high priority for many audio enthusiasts is the power output of their amplifiers. They want to get as much power as they can without high costs.

The two main factors affecting the amplifier power output are the available voltage supply and the circuit topology.

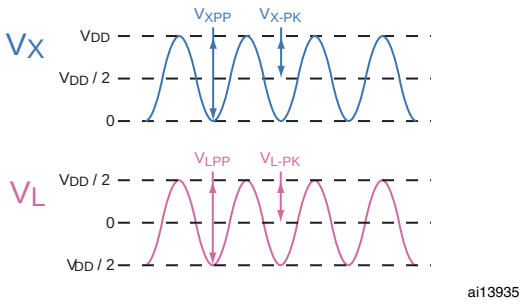
For a generic sinusoidal signal, the average power to the load is calculated as a function of the voltage. Either the peak-to-peak voltage, V_{PP} , or the peak voltage, V_{PK}, can be used. These are illustrated in *Figure 8*.

Figure 8. Voltage terminology



For the circuit in *Figure 7*, at maximum power, V_X will swing from V_{DD} to ground as shown in *Figure 9*. At the load, with the DC component removed, V_L will swing between $V_{DD}/2$ and $-V_{DD}/2$.

Figure 9. Simple amplifier outputs waveforms



The average or continuous power to a resistive load, R, for a sinusoidal signal, is

$$P_{AV} = \frac{V_{PK}^2}{2R} = \frac{V_{PP}^2}{8R}$$

This shows the power calculation using both the peak voltage V_{PK} and the peak-to-peak voltage V_{PP} .

For the circuit in *Figure 7*, the expression becomes

$$P_{L\text{-}AV} = \frac{V_{L\text{-}PK}^2}{2R_L} = \frac{V_{L\text{-}PP}^2}{8R_L}$$

At maximum swing, $V_{L\text{-}PK}$ equals $V_{DD}/2$, so the maximum continuous power to the load is

Equation 1

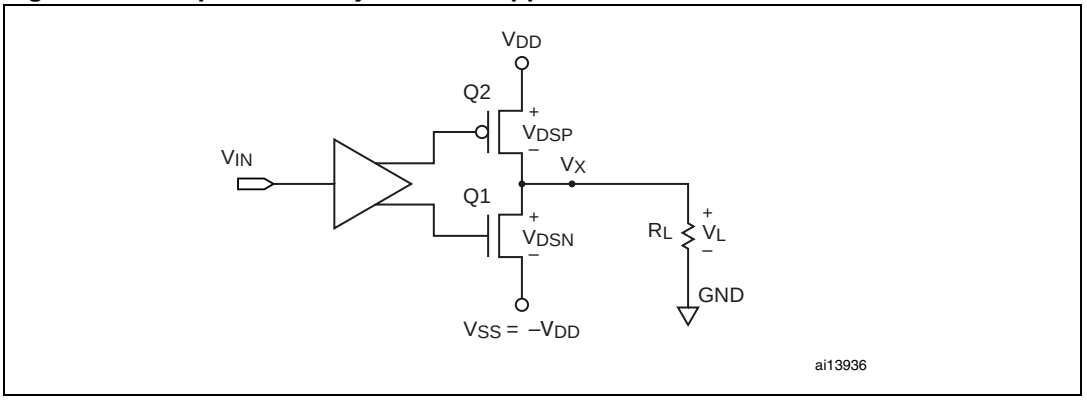
$$P_{L\text{-}AV\text{-}max} = \frac{V_{L\text{-}PK}^2}{2R_L} = \frac{(V_{DD}/2)^2}{2R_L} = \frac{V_{DD}^2}{8R_L}$$

Thus, for the topology in *Figure 7*, the power to the load is a function V_{DD} and R_L. To get more power to the load, the user must increase V_{DD} or decrease R_L, or use a different circuit topology.

2.2.3 Getting more power

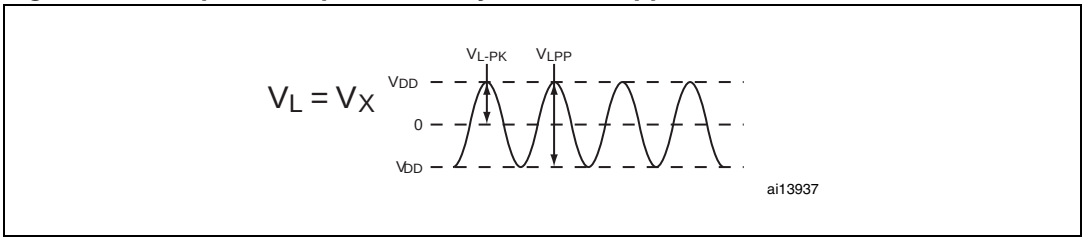
One technique for increasing the deliverable power is to add a negative supply equal in magnitude to the positive supply. This is depicted in *Figure 10*. With this addition, the midpoint, V_X, is at ground. One advantage of this is that no coupling capacitor is required thus removing any frequency roll off effects due to using an imperfect, real-world capacitor.

Figure 10. Amplifier with symmetric supplies



Thus, without the capacitor, $V_L = V_X$. For this topology, ignoring the V_{DS} drops in Q1 and Q2 as before, V_X will swing between V_{DD} and $-V_{DD}$ as shown in *Figure 11*.

Figure 11. Output of amplifier with symmetric supplies



As before, the continuous power to the load is

$$P_{L\text{-}AV} = \frac{V_{L\text{-}PK}^2}{2R_L}$$

At maximum continuous output power, $V_{L\text{-}PK}$ equals V_{DD}, so this becomes

$$P_{L\text{-}AV\text{-}max} = \frac{V_{L\text{-}PK}^2}{2R_L} = \frac{V_{DD}^2}{2R_L}$$

Thus, compared to *Equation 1*, by adding the negative supply, the maximum power increased by a factor of 4. The same effect could also be achieved by doubling V_{DD} in the circuit of *Figure 7*.

But either way, adding a supply or doubling the voltage can be costly. It is preferred to get the increase in power without such additional costs.

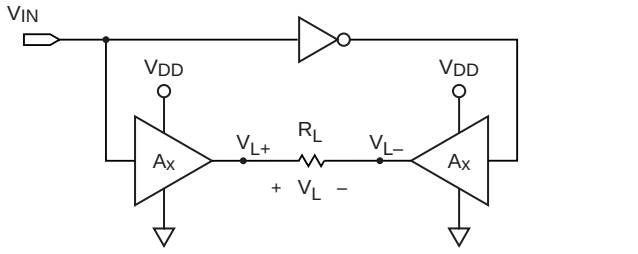
2.2.4 Bridged amplifiers

A bridged amplifier uses two identical amplifiers driven 180° out of phase. The circuit shown in *Figure 12* uses two single supply amplifiers, A_X. These would each be comparable to the amplifier of *Figure 7*.

The input signal is connected unchanged to the left amplifier and inverted prior to going to the right amplifier thus making the right one 180° out of phase with the left.

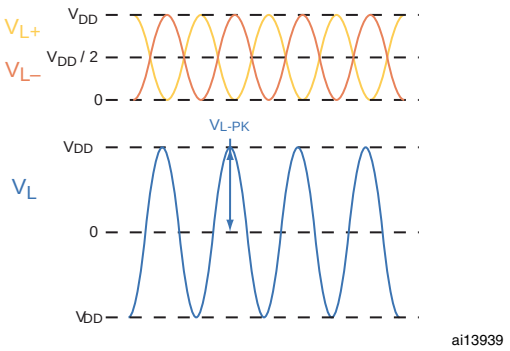
The outputs of the two amps, V_{L+} and V_{L-}, are each biased at $V_{DD}/2$. Thus, the quiescent difference between them is 0 V. Therefore, no DC blocking capacitor is required at the load.

Figure 12. Bridged amplifiers



Each output can swing between V_{DD} and ground as shown in *Figure 13*.

Figure 13. Outputs of bridged amplifier



At maximum swing, for sinusoidal outputs, V_{L+} and V_{L-} can be written as

$$V_{L+}(t) = \frac{V_{DD}}{2} \cdot \sin \omega t$$

and

$$V_{L-}(t) = \frac{V_{DD}}{2} \cdot \sin(\omega t - 180°) = -\frac{V_{DD}}{2} \cdot \sin \omega t = -V_{L+}$$

The load voltage, V_L, is the difference between the two outputs.

Equation 2

$$V_L = V_{L+} - V_{L-} = V_{L+} - (-V_{L+}) = 2V_{L+}$$

Thus, bridging has the effect of doubling the load voltage without adding or changing the voltage supply. In this example, the two amplifiers bridged together were each single supply devices, but dual-supply amplifiers such as that in *Figure 10* can also be bridged. The result will be the same - the deliverable load voltage will be double that of using a single amplifier.

2.2.5 Bridged power

For the circuit in *Figure 12*, the peak value of V_L is V_{DD} as shown in *Figure 13*. The maximum continuous power is then

$$P_{L\text{-}AV\text{-}max} = \frac{V_{L\text{-}PK}^2}{2R_L} = \frac{V_{DD}^2}{2R_L}$$

This is the same power as for the case of the dual-supply amplifier in *Figure 10*, and four times the power of that in *Figure 7*. By bridging two single-supply amplifiers, four times the power is available without the added cost of a second power supply. Hence, bridging is an economical and popular way of increasing amplifier power without expensive power supplies.

2.2.6 Automotive example

An automobile is a great example of the benefits of bridging. The standard supply of 12 V limits the load voltage unless an expensive DC-DC power supply is added to the system.

For the circuit of *Figure 7*, with V_{DD} = 12 V and an 8 ohm load, we get

$$P_{L\text{-}AV\text{-}max} = \frac{V_{DD}^2}{8R_L} = \frac{144}{64} = 2.25W$$

Thus, the maximum continuous power delivered to an 8 ohm speaker would be 2.25 W. Taking into account the V_{DS} drops in the drive transistors will further lower that. Conversely, most cars will be operating at a little more than 12 V, usually somewhere in the range 13.6 to 14.4 V, so that tends to offset the V_{DS} drops.

For the circuit of *Figure 12*, again with 12 V and 8 ohms, the power calculation is

$$P_{L\text{-}AV\text{-}max} = \frac{V_{DD}^2}{2R_L} = \frac{144}{16} = 9W$$

Bridging delivers 9 W, four times the previous case, as expected. And with a 4 ohm speaker, the load power goes up to 18 W.

For maximum power in the 12 V automotive environment, bridging offers a low cost alternative to expensive power supplies by increasing the available audio power by a factor of 4. Combined with 4-ohm speakers, users can achieve outstanding audio performance at moderate cost.

Similarly, in any environment where the voltage supply options are limited, bridging provides a significant power improvement for a nominal increase in silicon.

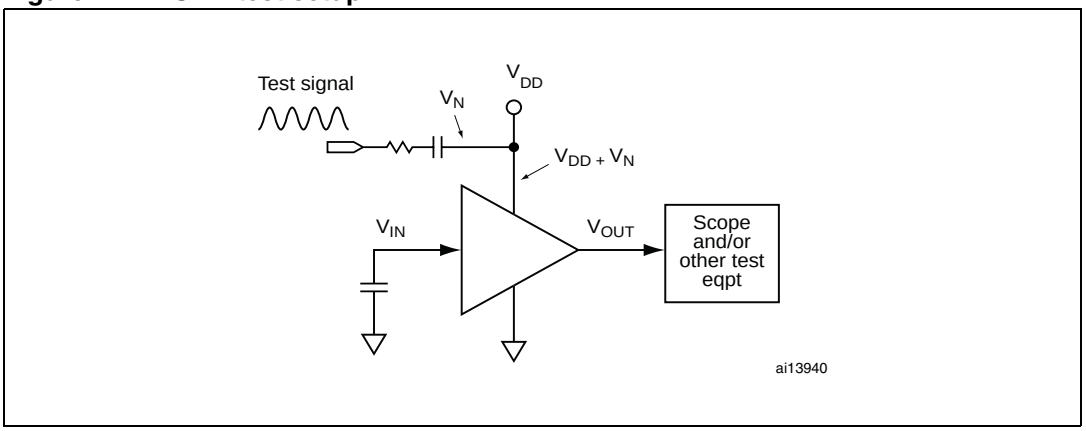
2.3 Power supply rejection ratio

The PSRR is a measure of how well the device keeps power supply noise out of its output. It is measured by setting the input to 0 and coupling a 200 mV_{PP} sign wave into V_{DD}.

The output signal is filtered to reject frequencies other than the test signal, in this case 1kHz. A fast fourier transform engine, or FFT, is helpful in implementing the filter and measuring the output level.

Since the PSRR is in the range of –55 to –65 dB, the output signal will be on the order of 200 uV. Without the FFT and filtering, the signal will be lost in the noise floor.

Figure 14. PSRR test setup



The PSRR is calculated as follows using the standard formula for power gain in dB.

$$PSRR = 20 \log (V_{OUT} / V_N)$$

Example:

If the output is measured as 350 uV, the PSRR will be

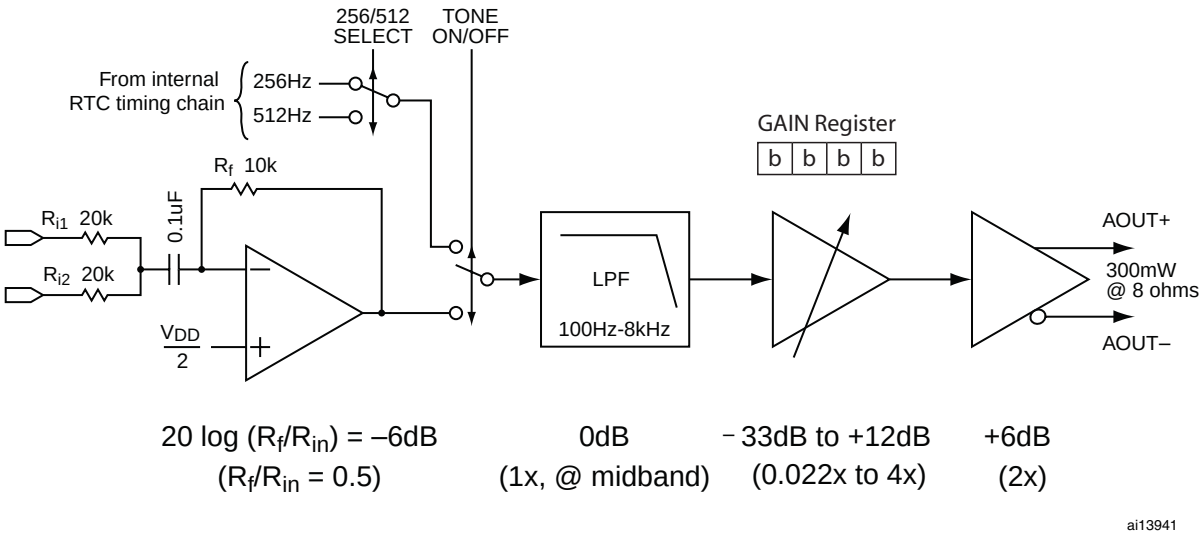
$$PSRR = 20 \log (350 u / 200 m) = –55.1 dB$$

2.4 Gain

There are three stages of gain in the M41T00AUD. The input amplifier's gain is controlled by the input and feedback resistors chosen by the user. The LPF is at unity gain and thus does not contribute.

The programmable gain stage can be adjusted from a gain (attenuation) of 0.022x all the way up to a 4x multiplication. Lastly, the bridge amplifier provides a fixed gain of 2x which is a consequence of two amplifiers in parallel, one at a gain of 1x and one at –1x, resulting in a net gain of 2 as shown in *Equation 2 on page 12*.

Figure 15. End-to-end audio path



The gain is usually measured in decibels or dB. This is defined as the ten times the log of the ratio of the output power to the input power

$$A_P = \text{power gain in dB} = 10\log\left(\frac{P_{OUT}}{P_{IN}}\right) = 10\log\left(\frac{V_{OUT}^2/R_{OUT}}{V_{IN}^2/R_{IN}}\right)$$

Normalizing the resistances, this reduces to

$$A_P = 10\log\left(\frac{V_{OUT}^2}{V_{IN}^2}\right) = 10\log\left(\frac{V_{OUT}}{V_{IN}}\right)^2 = 20\log\frac{V_{OUT}}{V_{IN}}$$

Example: In *Figure 15*, with $R_{in} = 2\ R_f$, the input gain is 0.5 which cancels out the final gain stage gain of 2. The net gain for these two sections is then 1. The result is that the final gain is determined solely by the adjustable gain stage and will match whatever value is programmed into the gain register.

3 M41T00 audio section specifications

In summary, the audio section of the M41T00AUD uses a bridged amplifier output stage which can deliver 300 mW into an 8 ohm load. The device produces less than 2% total harmonic distortion at this output level, typically 0.2%.

Signals are summed into the input by connecting multiple, parallel input resistors. For R_{in} = 20 k and C = 0.1 uF, the input will be attenuated below 80 Hz. The low pass filter after the input amplifier will attenuate signals above 8 kHz thus forming a band pass of 80 – 8000 Hz.

The end-to-end gain is controlled by the input and feedback resistors along with the software controlled gain stage. For $R_{in} = 2R_f$, software can adjust the gain between –33 and +12 dB. Lastly, with a PSRR of –55 dB, any noise present on the power supply will be reduced by at least 55 dB at the output.

4 Revision history

Table 1. Document revision history

Date	Revision	Changes
06-Dec-2007	1	Initial release.